REMARKS

STATUS SUMMARY

Claims 1-27 are pending in the present application. The Examiner has rejected claims 1-27 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,763,363 to *Driscoll* ("*Driscoll*").

These formal matters identified in the Office Action are addressed herein below.

RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1-27 are rejected under 35 U.S.C. § 102(e) as anticipated by *Driscoll*. Applicant respectfully traverses this rejection because *Driscoll* fails to teach each and every feature or element recited in the rejected claims.

Claim 1, as amended, of the present application recites the following:

> A system of digital data encryption in a digital device, comprising:
> an encryption key generator;
> a data buffer;
> an input/output register; and
> a memory controller that directs digital data to the data buffer with the digital data passing through the encryption key generator prior to entering the input/output register.

Specifically, *Driscoll* fails to teach "a memory controller that directs digital data to the data buffer with the digital data passing through the encryption key generator prior to entering the input/output register." In general, as its title indicates, *Driscoll* teaches "a computer efficient linear feedback shift register." The invention of *Driscoll* "provides a pseudo-random generator (PRNG) that includes a linear feedback shift register (LFSR) having a state." Col. 3: lines 46-48. With regard to the memory controller of claim 1 of the pending application, the Examiner cites col. 4: lines 30-46 of *Driscoll*:

> One form of a stream cipher cryptosystem according to the present invention includes a PRNG receiving a key and providing a keystream. The PRNG includes a word-by-word shifting LFSR according to the present invention for providing a LFSR output word of word length M. The stream cipher cryptosystem also includes a cryptographic combiner to provide a second binary data sequence. In encryption operations, the cryptographic combiner is an encryption combiner and the first binary data sequence is a plaintext binary data sequence and the second binary data sequence is a ciphertext binary data sequence. In decryption operations, the cryptographic combiner is a decryption combiner and the first binary data sequence is a ciphertext binary data numbers sequence and the second binary data sequence is a plaintext binary data sequence.

In general, what *Driscoll* teaches can be best summarized by its FIGs. 3 and 4. FIG. 3 illustrates a conventional bit-by-bit LFSR (col. 6: lines 48-49) while FIG. 4 generally illustrates a word-by-word left shifting LFSR according to the invention of *Driscoll*. (col. 7: lines 25-260) with the advantages of the latter LFSR described at col. 9: lines 14-52. Thus, in summary, all that *Driscoll* teaches is an improved, computer efficient, LFSR.

Therefore, contrary to the Examiner's assertion, *Driscoll* does not teach a memory controller that directs digital data to a data buffer where the digital then passes through an encryption key generator prior to entering an input/output register. In general, the pending application relates to methods and systems that "provide data encryption and decryption at the memory interface in a digital device." *See specification*, page 2, **[007]**, lines 1-2. In an example implementation, an encryption circuit is placed between a data buffer and an input/output register (*specification*, page 4, **[019]**, lines 1-2) and digital data ready for encryption is moved through the encryption circuit to the input/output register under the control of the memory controller (*specification*, page 4, **[020]**, lines 1-3). There is nothing in *Driscoll* that teaches or suggests the placement of an encryption circuit having LFSRs with respect to the memory interface in a digital device.

Independent claim 9, as amended, is a claim that includes "a memory controller that sends a memory request," and independent claim 25, as amended, recites a set-top box apparatus that includes "a memory controller that directs the storage of the digital data in the rewritable memory." Independent method claim 12 includes the step of encrypting digital data using a key while the digital data is being placed in a rewritable memory and independent method claim 22 includes the step of generating a memory request to retrieve encrypted digital data.

Thus these remaining independent claims 9, 12, 22, and 25 each include similar limitations as found in claim 1 and these claims are therefore also patently distinct from *Driscoll* for at least the same reasons. In general, that limitation is a memory controller capable of generating a memory control signal that is used to write digital data to rewriteable memory after that digital data is encrypted in an encryption circuit, and that limitation is not taught by *Driscoll*. *Driscoll* therefore fails to teach each and every feature or element recited in each of independent claims 1, 9, 12, 22, and 25.

Accordingly, applicant believes that independent claims 1, 9, 12, 22, and 25 are in condition for allowance and because all other claims are dependent directly or indirectly from allowable claims 1, 9, 12, 22, and 25, applicant respectfully request that the Examiner withdraw the rejection of claims 1-27 under 35 U.S.C. § 102(e).

CLAIM AMENDMENTS

Amendments have been made to claims 1, 2, 4-10, 13-15, 17-21, 23-25, and 27 to improve grammar and clarity, to correct typos, and to correct a lack of antecedent basis in certain claims. For example, claims 7, 14, 17, and 21 have been amended to change their dependencies.

Claim 1 has been amended to provide an antecedent basis for the input/output register, and claims 6, 8, 10, and 27 also correct a lack of antecedent basis. Claims 5 and 14 have been amended to correct spelling errors and claims 15, 17-21, 23, and 24 have been amended to improve readability.

None of the amendments to the claims discussed in this section have been made in response to a substantive rejection or for any other purpose relating to patentability, and the amendments made to the claims are believed to be fully supported by the present application as originally filed. Accordingly, no new matter is believed to have been added by these amendments.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

Respectfully submitted,
Winefred Washington

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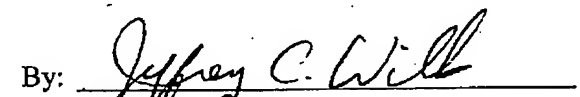
By: 

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